Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **INPUT FREQ COMP A**
2. **- INPUT**
3. **+ INPUT**
4. **V –**
5. **OUTPUT FREQ COMP**
6. **OUTPUT**
7. **V +**
8. **INPUT FREQ COMP B**

**.038”**

**1**

**2**

**3**

**4 5 6 7**

**8**

**MASK**

**REF**

**.038”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” x .004” min.**

**Backside Potential: V-**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .038” X .038” DATE: 4/27/23**

**MFG: FAIRCHILD THICKNESS .014” P/N: UA709**

**DG 10.1.2**

#### Rev B, 7/19/02